

FIG. 1

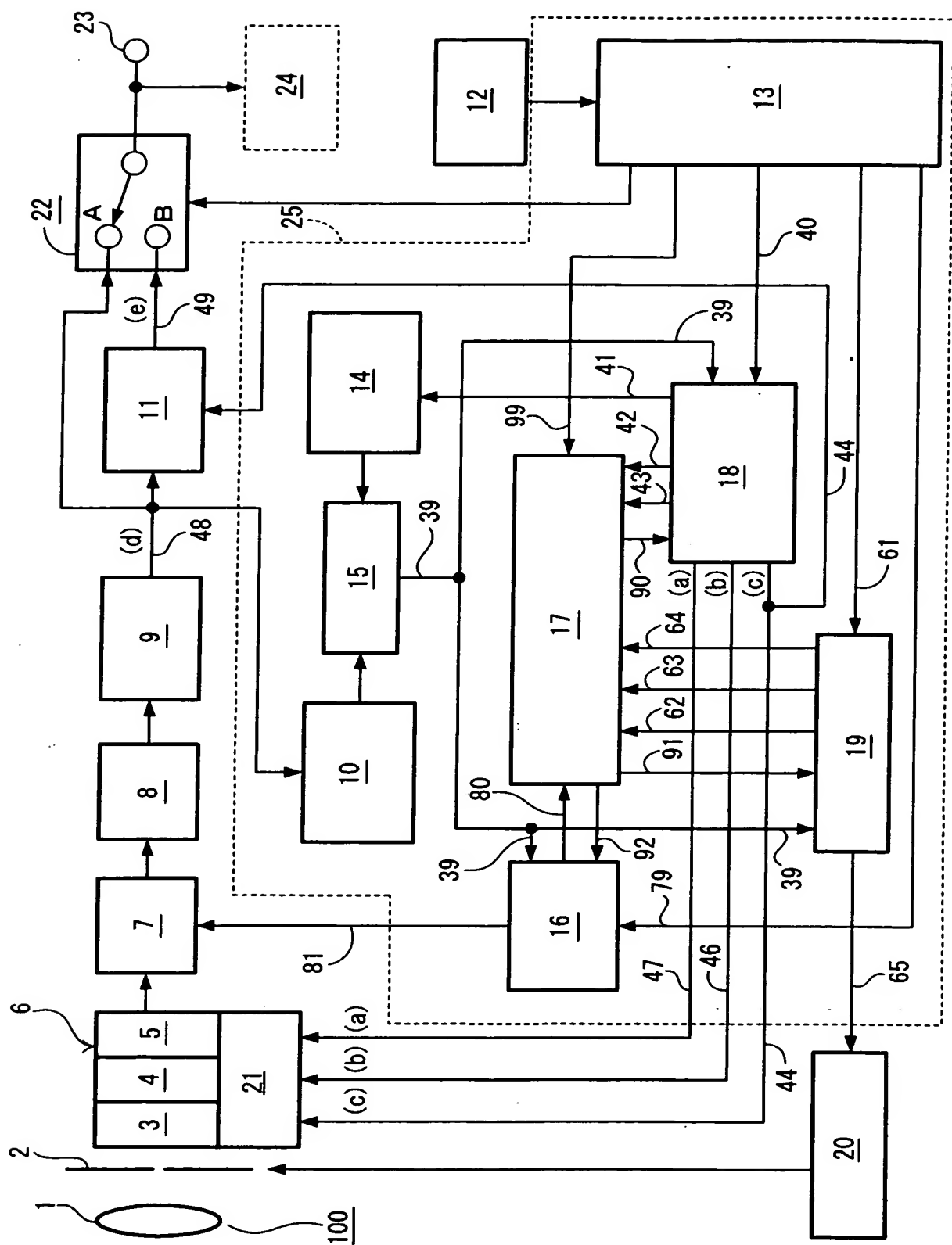


FIG. 2

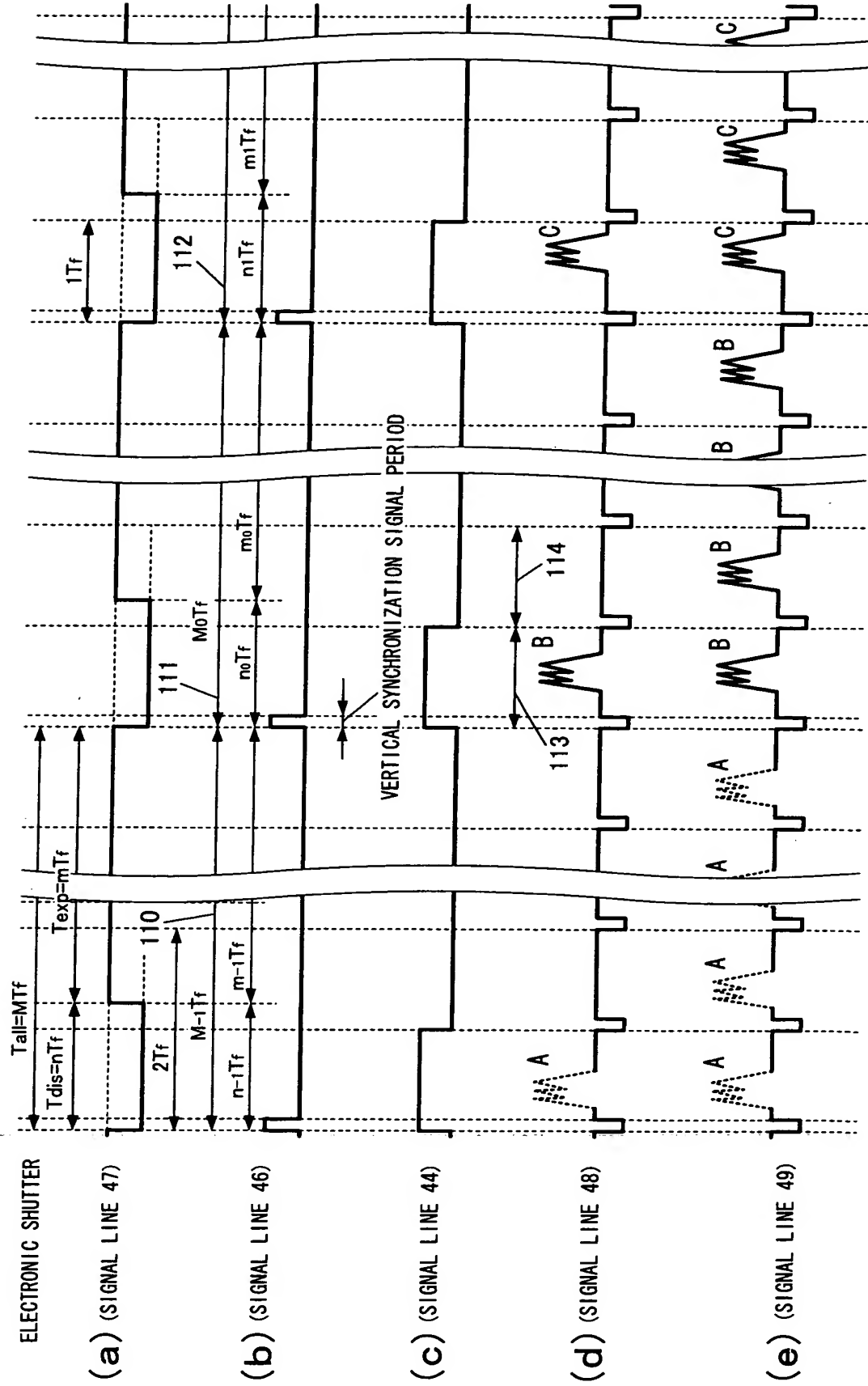


FIG. 3

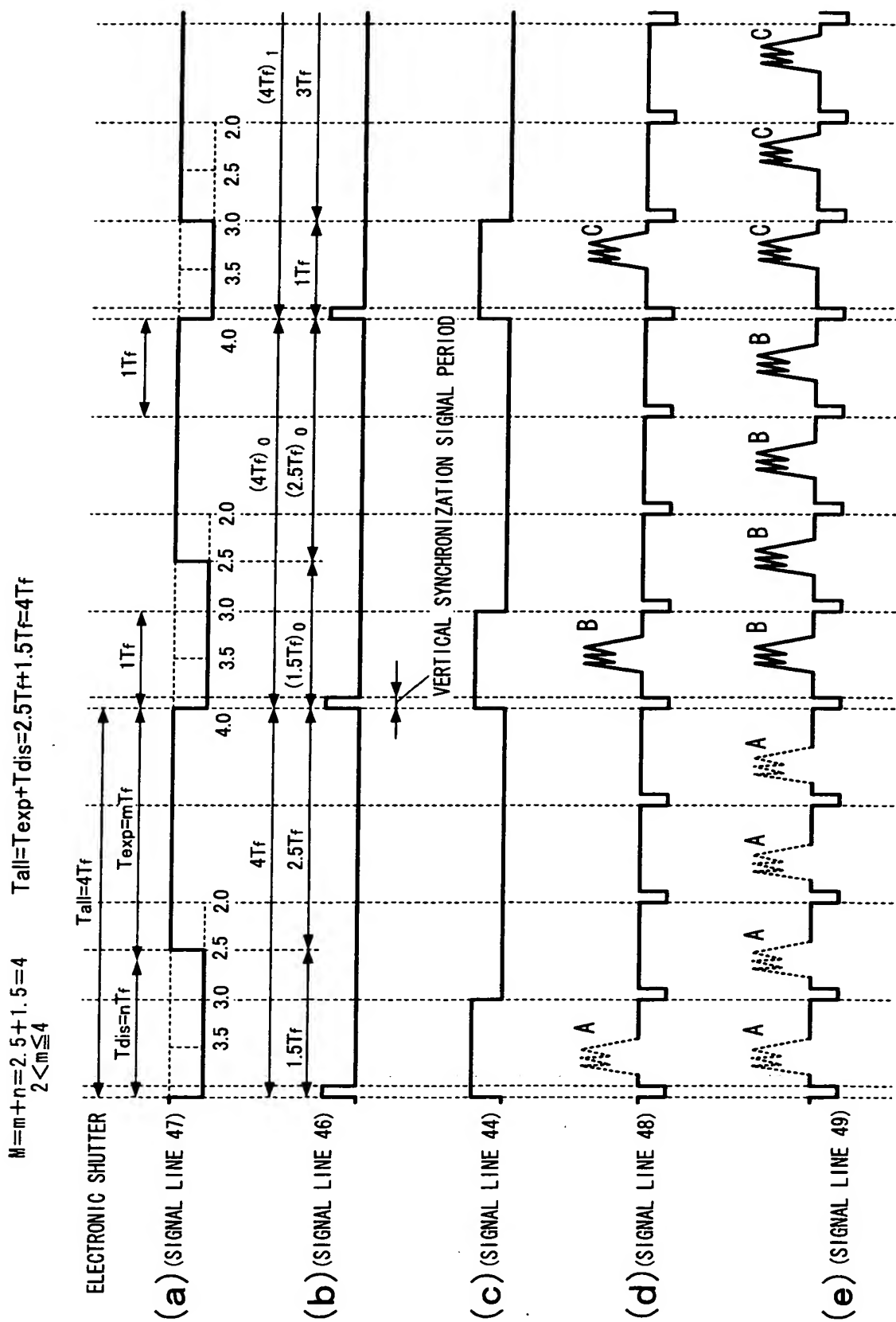


FIG. 4

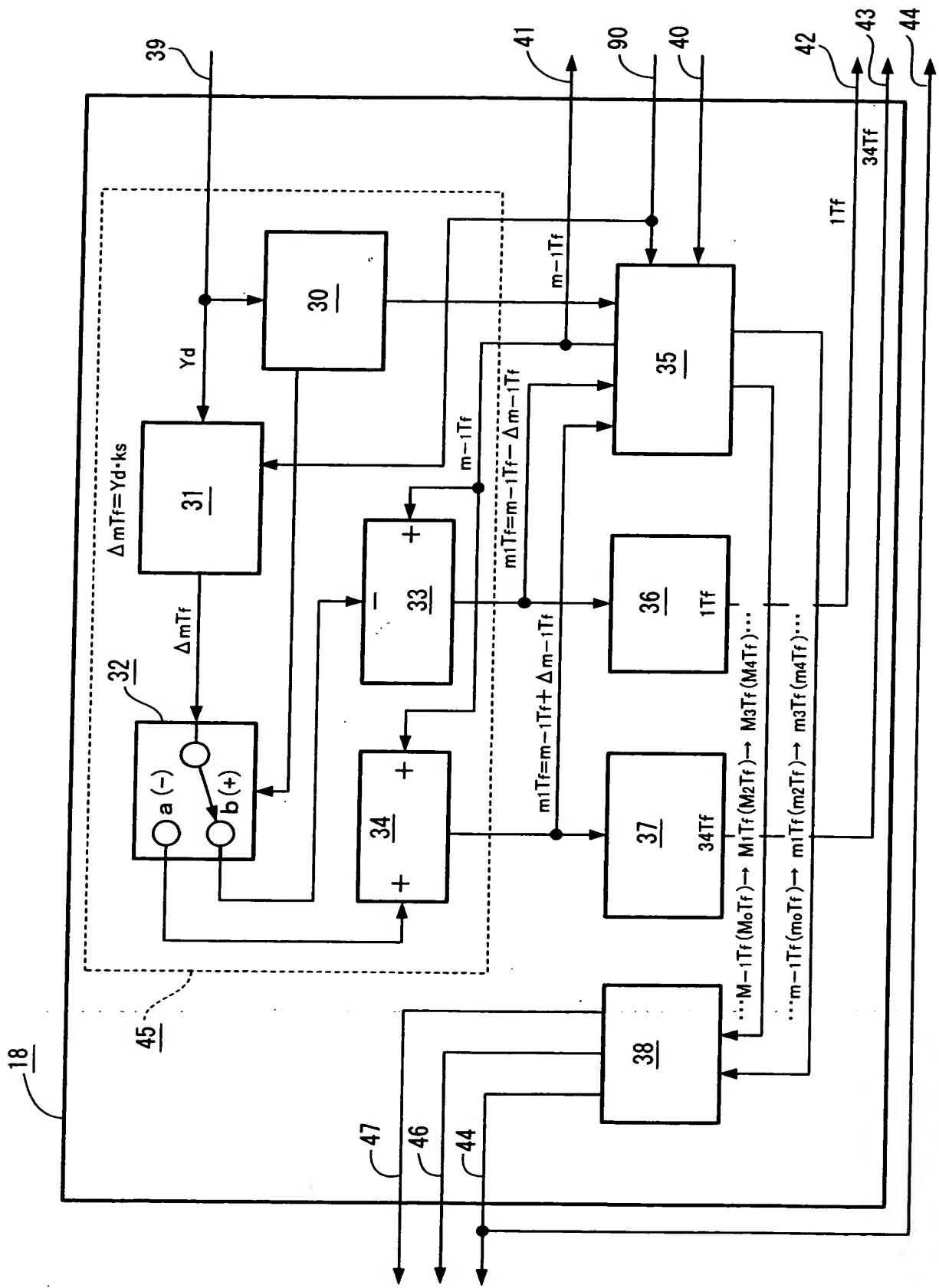


FIG. 5

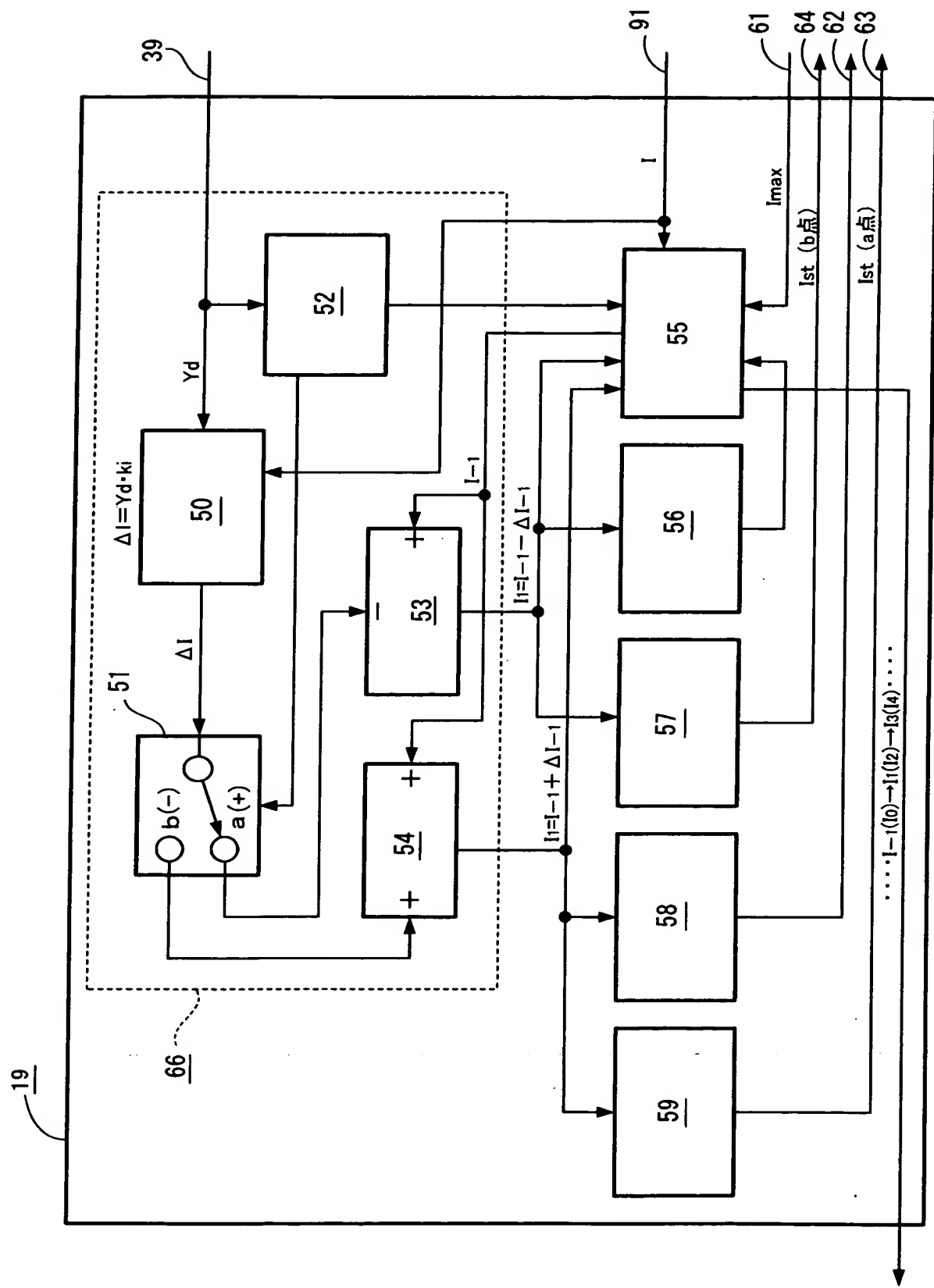


FIG. 6

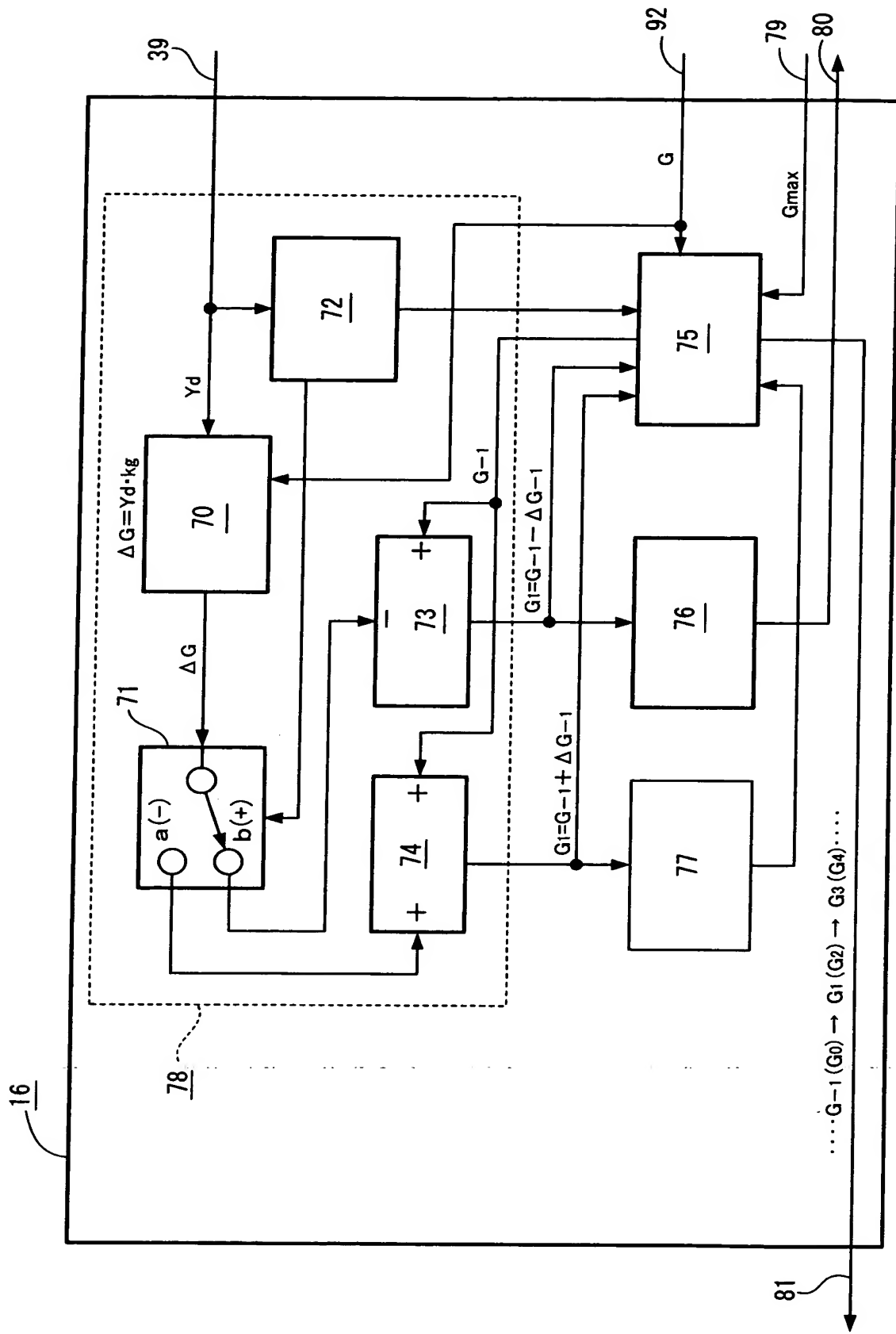
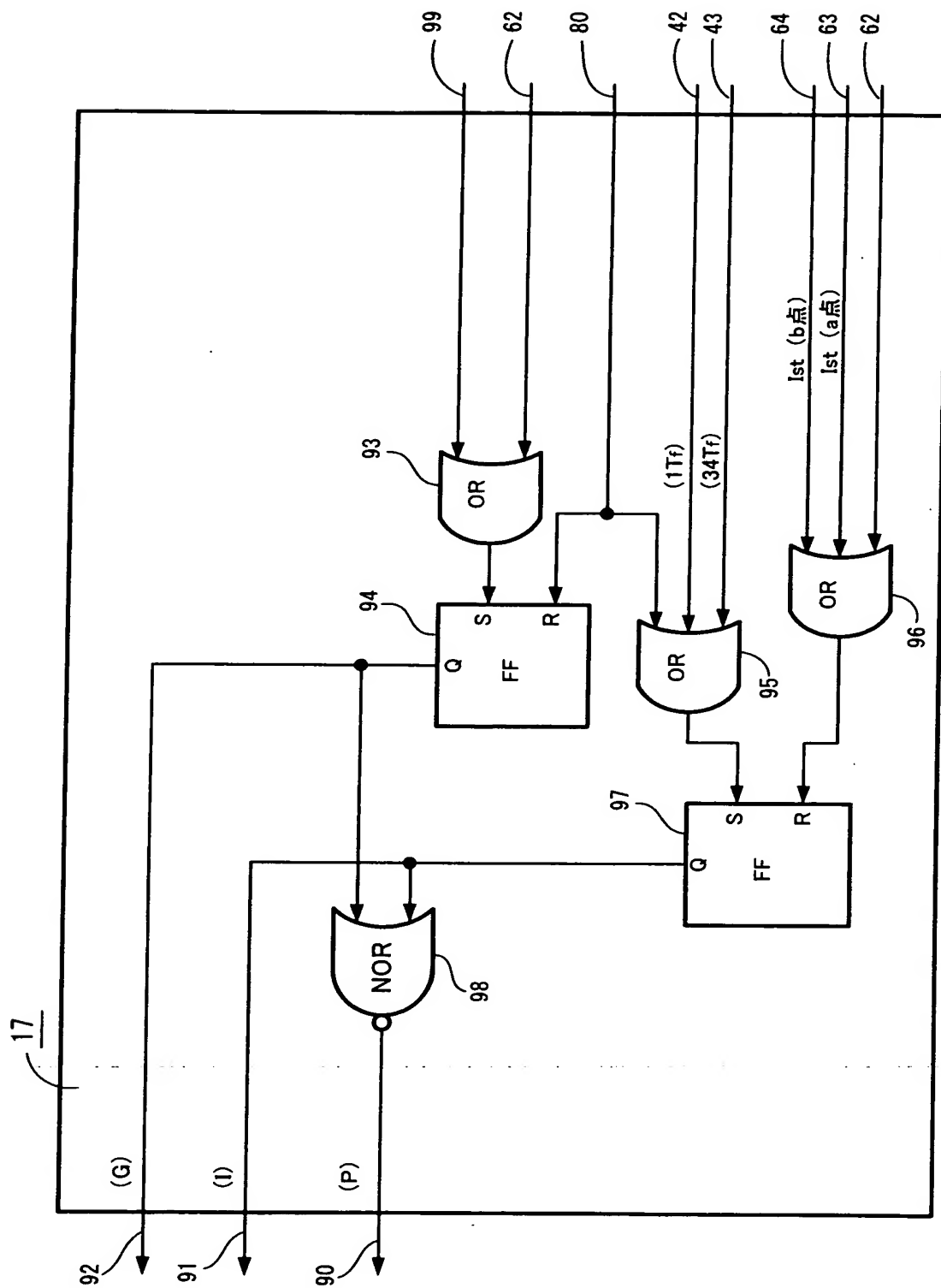


FIG. 7



Timing diagram for the 74LS148 3-to-8 decoder. The diagram shows the timing relationships between the three inputs (A, B, C), the three outputs (D, E, F), and the three enable inputs (G, H, I). The inputs are active-low, and the outputs are active-low. The enable inputs are active-low. The diagram is divided into seven sections labeled (a) through (g). Section (a) shows the timing for the first output (D) when the inputs are 000. Section (b) shows the timing for the second output (E) when the inputs are 001. Section (c) shows the timing for the third output (F) when the inputs are 010. Section (d) shows the timing for the fourth output (G) when the inputs are 011. Section (e) shows the timing for the fifth output (H) when the inputs are 100. Section (f) shows the timing for the sixth output (I) when the inputs are 101. Section (g) shows the timing for the seventh output (J) when the inputs are 110. The diagram also shows the timing for the eighth output (K) when the inputs are 111. The timing is shown for a clock period of 10 ns. The diagram is labeled 'TIMING DIAGRAM' at the top and '74LS148' at the bottom.

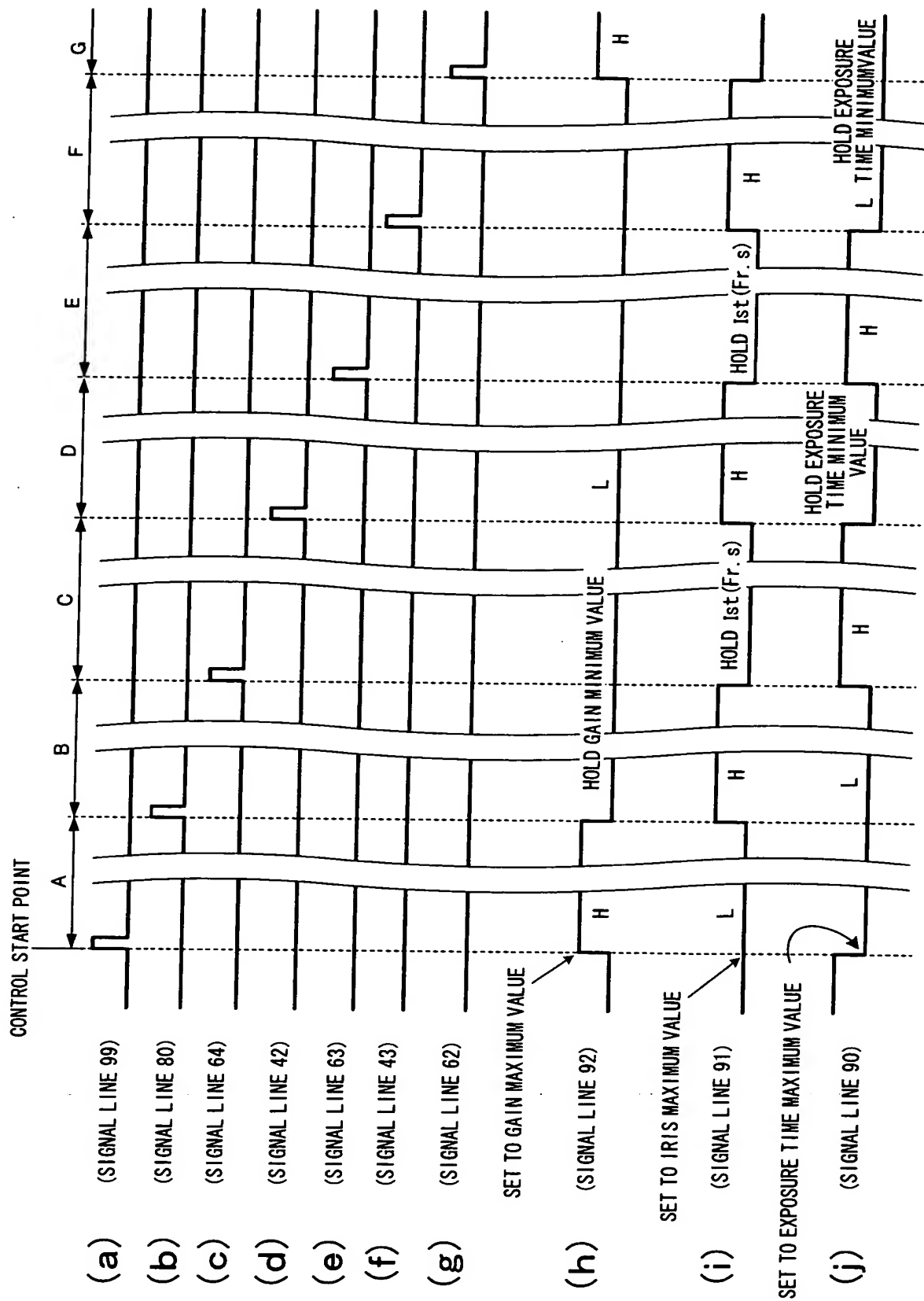




FIG. 9

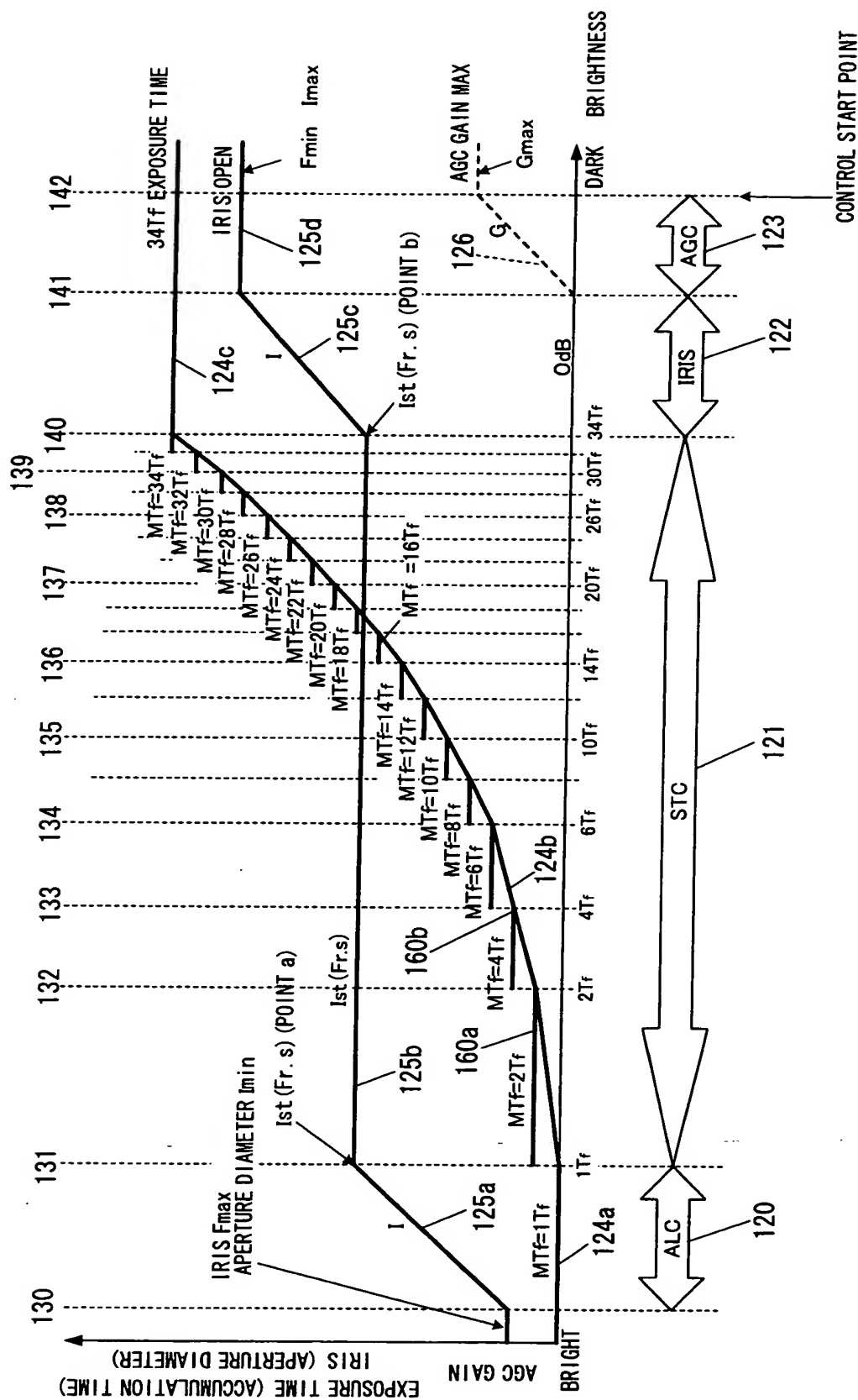


FIG. 10

